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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,768	CHAE, GEE SUNG	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/28/04 has been entered.

Product-by-Process Limitations

2. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes

clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art figure 4B.

Applicant's admitted prior art figure 4B discloses a liquid crystal display device comprising:

a substrate 1;

a gate electrode 3 over the substrate;

a first semiconductor layer 15 over the substrate; and

a source electrode 6a,6b (right portion) and a drain electrode 6a,6b (left portion) over the first semiconductor layer 15, the source and drain electrodes having a first metal layer 6a and a second metal layer 6b formed in a same pattern and defining a separation between the source electrode 6a,6b (right portion) and drain electrode 6a,6b (left portion) and side-walls of the first and second metal layers are substantially aligned.

The limitation of the first metal layer being patterned by dry etching process using the second metal layer as a mask is a product-by-process limitation that does not structurally distinguish over the prior art. The first and second metal layers are disclosed as being in the same pattern with substantially aligned side-walls and thus reads on the structure as claimed regardless of the method by which it was fabricated.

With regard to claim 3, the first metal layer includes molybdenum or titanium.

With regard to claim 4, the second metal layer includes aluminum or copper.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figure 2, in view of Ueda et al. (U.S. Patent No. 6,078,365).

With regard to claim 1, Applicant's admitted prior art figure 2 teaches a liquid crystal display device comprising:

a substrate 1;

a gate electrode 3 over the substrate;

a first semiconductor layer 15 over the substrate; and

a source electrode 5 and a drain electrode 7 over the first semiconductor layer 15, the source and drain electrodes having a first metal layer and being formed in a pattern that defines a separation between the source electrode and drain electrode.

The limitation of the first metal layer being patterned using the second metal layer as a mask is a product-by-process limitation that does not structurally distinguish over the prior art. The first and second metal layers are disclosed as being in the same pattern and thus reads on the structure as claimed regardless of the method by which it was fabricated.

Applicant's admitted prior art figure 2 does not teach the source and drain electrodes having a first metal layer and a second metal layer formed in a same pattern as the first metal layer and defining a separation between the source and drain electrodes with side-walls of the first and second metal layer being substantially aligned.

Ueda et al. teach a liquid crystal display device in figure 15f, for example. Ueda et al. teach source and drain electrodes 79 formed above a semiconductor layer 77, the source and drain electrodes having a first metal layer and a second metal layer, the first and second metal layer having the same pattern and defining a separation between the source electrode and drain electrode and having side-walls substantially aligned. Ueda teach the source and drain electrodes 79 having a first and second metal layer on column 17 lines 22-30 where layer 79 is a three-layered structure.

Applicants admitted prior art figure 2 and Ueda et al. are combinable because they are from the same field of endeavor. At the time of the invention, it would have

been obvious to one of ordinary skill in the art to form the source and drain electrodes from the three-layered structure of Ueda et al. (which includes the first and second metal layers as claimed). The motivation for doing so is to include aluminum in the electrodes to lower their resistance for improved conductivity of the circuit components. Therefore, it would have been obvious to combine Applicant's admitted prior art figure 2 with Ueda et al. to obtain the invention of claim 1.

The limitation of the first metal layer being patterned by dry etching process using the second metal layer as a mask is a product-by-process limitation that does not structurally distinguish over the prior art. The first and second metal layers are disclosed as being in the same pattern with substantially aligned side-walls and thus reads on the structure as claimed regardless of the method by which it was fabricated.

With regard to claim 2, Applicant's admitted prior art further teaches a gate insulating film 9 over the gate electrode and between the substrate and the first semiconductor layer; a second semiconductor layer 17 between the first metal layer and the first semiconductor layer, the second semiconductor layer defining a portion of the separation region in the same pattern as the first metal layer, a protective layer 21 over the source and drain electrodes, and a pixel electrode 23 provided over the protective layer. In combination with Ueda et al., the second semiconductor layer is also in the same pattern as the second metal layer as Ueda et al. teach the first and second metal layers having the same pattern.

With regard to claim 3, the first metal layer of Applicant's admitted prior art is molybdenum.

With regard to claim 4, the second metal layer of Ueda et al. is aluminum.

With regard to claim 5, Applicant's admitted prior art figure 2 teaches a liquid crystal display device comprising:

a substrate 1;

a gate electrode 3 over the substrate;

a first semiconductor layer 15 over the substrate;

a source electrode 5 and a drain electrode 7 over the first semiconductor layer 15, the source and drain electrodes having a first metal layer and being formed in a pattern that defines a separation between the source electrode and drain electrode, and a second semiconductor layer 17 beneath the first metal layer and having the same pattern as the first metal layer.

Applicant's admitted prior art figure 2 does not teach the source and drain electrodes having a first metal layer and a second metal layer formed in a same pattern as the first metal layer and defining a separation between the source and drain electrodes where sidewalls of the first and second metal layers are substantially aligned.

Ueda et al. teach a liquid crystal display device in figure 15f, for example. Ueda et al. teach source and drain electrodes 79 formed above a semiconductor layer 77, the source and drain electrodes having a first metal layer and a second metal layer, the first and second metal layer having the same pattern and defining a separation between the source electrode and drain electrode and the first and second metal layer having sidewalls that are substantially aligned. Ueda teach the source and drain electrodes 79

having a first and second metal layer on column 17 lines 22-30 where layer 79 is a three-layered structure.

Applicants admitted prior art figure 2 and Ueda et al. are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the source and drain electrodes from the three-layered structure of Ueda et al. (which includes the first and second metal layers as claimed). The motivation for doing so is to include aluminum in the electrodes to lower their resistance for improved conductivity of the circuit components. Therefore, it would have been obvious to combine Applicant's admitted prior art figure 2 with Ueda et al. to obtain the invention of claim 5.

The limitation of the first metal layer being patterned by dry etching process using the second metal layer as a mask is a product-by-process limitation that does not structurally distinguish over the prior art. The first and second metal layers are disclosed as being in the same pattern with substantially aligned side-walls and thus reads on the structure as claimed regardless of the method by which it was fabricated.

With regard to claim 6, Applicant's admitted prior art figure 2 further teaches a gate insulating film 9 over the gate electrode, a protective layer 21 over the source and drain electrodes, and a pixel electrode 23 provided over the protective layer

With regard to claim 7, the first metal layer of Applicant's admitted prior art figure 2 is molybdenum.

With regard to claim 8, the second metal layer of Ueda et al. is aluminum.

With regard to claims 21 and 22, the source and drain electrodes 79 of Ueda et al. are taught as a three-layer structure on column 17 lines 22-30. In this three layer structure the top layer is considered an ohmic contact layer. This ohmic contact layer is over the first semiconductor layer and inner edges of the ohmic contact layer facing the separation space are aligned with inner edges of the first metal layer. This is shown in Ueda et al. figure 15f where the three layer structure 79 has the same structure throughout.

With regard to claim 23, Applicant's admitted prior art figure 2 teaches a liquid crystal display device comprising:

a substrate 1;

a gate electrode 3 over the substrate;

a first semiconductor layer 15 over the substrate; and

a source electrode 5 and a drain electrode 7 over the first semiconductor layer 15, the source and drain electrodes having a first metal layer and being formed in a pattern that defines a separation between the source electrode and drain electrode.

Applicant's admitted prior art figure 2 does not teach the source and drain electrodes having a first metal layer and a second metal layer formed in a same pattern as the first metal layer and defining a separation between the source and drain electrodes where sidewalls of the first and second metal layers are substantially aligned. Applicant's admitted prior art also do not teach an ohmic contact layer over the first semiconductor layer wherein inner edges of the ohmic contact layer facing the separation space are aligned with inner edges of the first metal layer.

Ueda et al. teach a liquid crystal display device in figure 15f, for example. Ueda et al. teach source and drain electrodes 79 formed above a semiconductor layer 77, the source and drain electrodes having a first metal layer and a second metal layer, the first and second metal layer having the same pattern and defining a separation between the source electrode and drain electrode and the first and second metal layer having sidewalls that are substantially aligned. Ueda teach the source and drain electrodes 79 having a first and second metal layer on column 17 lines 22-30 where layer 79 is a three-layered structure. In this three layer structure the top layer is considered an ohmic contact layer. This ohmic contact layer is over the first semiconductor layer and inner edges of the ohmic contact layer facing the separation space are aligned with inner edges of the first metal layer. This is shown in Ueda et al. figure 15f where the three layer structure 79 has the same structure throughout.

Applicants admitted prior art figure 2 and Ueda et al. are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the source and drain electrodes from the three-layered structure of Ueda et al. (which includes the first and second metal layers as claimed). The motivation for doing so is to include aluminum in the electrodes to lower their resistance for improved conductivity of the circuit components. Therefore, it would have been obvious to combine Applicant's admitted prior art figure 2 with Ueda et al. to obtain the invention of claim 23.

The limitation of the first metal layer being patterned by dry etching process using the second metal layer as a mask is a product-by-process limitation that does not

structurally distinguish over the prior art. The first and second metal layers are disclosed as being in the same pattern with substantially aligned side-walls and thus reads on the structure as claimed regardless of the method by which it was fabricated.

With regard to claim 24, Applicant's admitted prior art further teaches a gate insulating film 9 over the gate electrode and between the substrate and the first semiconductor layer; a second semiconductor layer 17 between the first metal layer and the first semiconductor layer, the second semiconductor layer defining a portion of the separation region in the same pattern as the first metal layer, a protective layer 21 over the source and drain electrodes, and a pixel electrode 23 provided over the protective layer. In combination with Ueda et al., the second semiconductor layer is also in the same pattern as the second metal layer as Ueda et al. teach the first and second metal layers having the same pattern.

With regard to claim 25, the first metal layer of Applicant's admitted prior art is molybdenum.

With regard to claim 26, the second metal layer of Ueda et al. is aluminum.

Response to Arguments

7. Applicant's arguments filed 7/28/04have been fully considered but they are not persuasive.

With regard to the use of figures 2, 4A and 4B as admitted prior art, Applicant argues that the examiner has not met the burden of establishing a prima facie case that the figures are prior art. These figures have been treated as admitted prior art. The

figures are labeled "conventional" and are discussed in the "background of the invention" section of the application. Labeling the figures as "conventional" and discussing them in the "background" is considered sufficient evidence that these figures are prior art. In support of this we need look no further than the definition of "conventional" and "background". According to Webster's Collegiate Dictionary, tenth edition, "conventional" means "2 a: according with, sanctioned by, or based on convention; b: lacking originality or individuality; c: ordinary, commonplace; 3 b: of traditional design." "Background" is defined as "b (1): the circumstances or events antecedent to a phenomenon or development." Thus, labeling the figure as "conventional" and discussing the figures in the "background" sufficient evidence has been presented that the figures are indeed prior art to the applicant's invention and the examiner's initial burden has been met.

Applicant also presents arguments that since the "admitted prior art" has allegedly not been established as prior art, no prior art has been established for Ueda et al. to modify. This is not persuasive as the examiner has met the burden of establishing that figure 2 of applicant's specification is admitted prior art and thus a proper rejection has been established.

Applicant also argues that figure 2 does not indicate a problem that would need the improved conductivity of its components (taken from the examiners motivation to combine Ueda et al. in which the electrode structure of Ueda et al. is provided to lower resistance by allowing the use of aluminum in the three-layer structure). This is not persuasive as figure 2 (admitted prior art) does not need to recognize a problem and the

combination is proper so long as there is some stated motivation or reasoning in the references. Ueda et al. explicitly states that Mo and Al are used to decrease the electrical resistance of the metal film.

Applicant further states that layer 79 of Ueda et al. is disclosed to be transparent but aluminum is not transparent so that the alleged motivation is taught away from by Ueda et al. This is not persuasive as Ueda et al. clearly teaches aluminum as part of layer 79. It is not clear where Ueda et al. teaches that layer 79 needs to be transparent. If Ueda et al. discusses layer 79 being transparent in a different embodiment it is irrelevant to the rejection.

Third, Applicant argues that Ueda et al. discloses their layers 79, 78, 77 and 76 patterned in "almost the same shape" and as such does not teach the (second) semicondouctor layer having the same pattern as the first metal layer. This is not persuasive as Ueda et al. was not relied upon to teach the second semiconductor layer having the same pattern as the first metal layer. Admitted prior art figure 2 was relied upon to teach the source electrode 5 and drain electrode 7 patterned to form a separation region and the second semiconductor layer 17 beneath the electrodes having a same pattern as the electrodes. Ueda et al. was relied upon to teach the multilayer electrode. Thus, the rejection is considered proper as admitted prior art figure 2 shows the claimed limitation. Further, even though Ueda et al. shows in figure 15f might be construed to show "almost the same pattern" for layers 79, 78, 77 and 76, as shown layer 19 has the same pattern throughout such that in combining the three-

layer electrode of Ueda et al. into the admitted prior art figure 2, all three layers would have the same pattern as the second semiconductor layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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